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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/322,708	05/28/1999	KIRK DOW SANDERS	81862.P125	8389

8791 7590 06/13/2003

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EXAMINER	
HO, DUC CHI	

ART UNIT	PAPER NUMBER
2665	9

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPG

Office Action Summary	Application No. 09/322,708	Applicant(s) SANDERS ET AL.	
	Examiner Duc C Ho	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-9 and 30-37* is/are allowed.

6)☐ Claim(s) *1-5 and 10-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 10-15 are withdrawn in view of the newly discovered reference(s) to Koenig et al., Yamashita and the admitted prior art in figure 2 of the instant application. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4, 10-13, 16-19, 21-23, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamashita, in view of the admitted prior art in figure 3 of the instant application.

Regarding claim 1, Yamashita discloses a path-monitoring system for cross-connect system.

receiving a time division multiplexed (TDM) stream on an input of the transmission system (the digital cross-connect system receives a plurality of TDM input lines #1- #N (see figure 3, column 2, lines 53-65). Each TDM frame or TDM stream contains N idle timeslots and data timeslots (column 1, lines 64-68)) *wherein the TDM stream comprises a plurality of data fields* (data timeslots) *and a plurality of unused fields* (idle timeslots)*;*

inserting test data in one or more of the plurality unused fields of the TDM stream (each test pattern insertion circuits 30_1 - 30_N, fig. 3 inserts a test pattern into idle timeslot of one of N successive frames (column 1, lines 65-67, and column 3, lines 41-50));

transferring the TDM stream along a plurality of components of the transmission system (the TDM frame containing idle timeslot and data timeslot is cross-connected or transferred along from the input to the output via a plurality of insertion circuits 30_1 - 30_N, RAM 40_1 - 40_N, and check circuit 32_1 - 32_N)*; and*

comparing the test data (the inserted test pattern or the original pattern) *against the transferred data* (test pattern) (each check circuit 32_1 - 32_N determines whether each test pattern matches the original pattern, column 2, lines 56-60).

Yamashita, however, does not teach the time slot interchangers (TSIs) to couple between the input lines and the output lines of the cross connect system.

TSI is well known in the art for connecting any time slot of an incoming TDM stream to a different time slot of an outgoing TDM stream.

The admitted prior art in figure 1 discloses a TSI coupled between the framers and the banks of DSPs. In general, a plurality of TSIs can also be used in system 100 for switching a time slot from the incoming TDM stream to a different time slot of the outgoing TDM stream.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ time slot interchangers as taught by the admitted prior art in figure 3 of the instant application into the system of Yamashita with the motivation is that any time slot of an incoming TDM frame could be connected to a different time slot of an outgoing TDM stream.

Regarding claim 2, in Yamashita a plurality of connection paths (#1-N) are established through insertion circuits 30_1 - 30_N, time switch 31_1 -31_N, and output line #1-N, figure 3.

Regarding claim 3, in Yamashita each insertion circuit 30_1 -30_N inserts a test pattern A into a single time slot of frame #K (column 3, lines 37-50), and the test data is configured to transfer along the connection paths and circuits described in claim 2.

Regarding claim 4, in Yamashita test patterns A is inherently stored in each insertion circuit 30_1 -30_N.

Regarding claim 10, Yamashita in figure 3, column 3, lines 41-44, discloses a selector 34 (*a controller*), a timing generator 37 and a frame counter 38 (a framer block), wherein each frame includes idle time slots and data time slots, and insertion circuits (a logic circuit) for inserting test pattern into idle time slot of a frame.

Yamashita, however, does not teach (1) the time slot interchangers (TSIs) to couple between the input lines and the output lines of the cross connect system, and (2) the controller for setting up connections between interfaces of the transmission system.

TSI is well known in the art for connecting any time slot of an incoming TDM stream to a different time slot of an outgoing TDM stream.

The admitted prior art in figure 1 discloses (2) a controller 170 for setting up or tearing down the call connections (page 3, lines 1015), and (1) a TSI coupled between the framers and

the banks of DSPs. In general, a plurality of TSIs can also be used in system 100 for switching a time slot from the incoming TDM stream to a different time slot of the outgoing TDM stream.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ a controller for setting up and tearing down a call connection, and time slot interchangers as taught by the admitted prior art in figure 3 of the instant application into the system of Yamashita with the motivation is that to control a call's establishment and a call's ending and any time slot of an incoming TDM frame could be connected to a different time slot of an outgoing TDM stream in order to meet the required speed and efficiency of a telecommunication network.

Regarding claim 11, please see the rejection of claim 10. The TSI is considered as one among other circuits for transferring test pattern in an idle time slot.

Regarding claim 12, the insertion circuit inherently includes a receiver for storing the transferred test pattern.

Regarding claim 13, the insertion circuit 30 and the check circuit 32 are configured for testing the system. The check circuit inherently includes a comparator for checking each test pattern against the original single test pattern, column 3, lines 57-60.

Regarding claim 16, Yamashita in figure 3, column 3, lines 41-44, discloses a selector 34 (*a controller*), a timing generator 37 and a frame counter 38 (a framer block), wherein each frame includes idle time slots and data time slots, and insertion circuits (a logic circuit) for inserting test pattern into idle time slot of a frame, wherein as a part of the system configured for testing the system, the check circuit 32 inherently includes a comparator for checking each test pattern against the original single test pattern, column 3, lines 57-60.

Yamashita, however, does not teach (1) the time slot interchangers (TSIs) to couple between the input lines and the output lines of the cross connect system, and (2) the controller for setting up connections between interfaces of the transmission system.

TSI is well known in the art for connecting any time slot of an incoming TDM stream to a different time slot of an outgoing TDM stream.

The admitted prior art in figure 1 discloses (2) a controller 170 for setting up or tearing down the call connections (page 3, lines 1015), and (1) a TSI coupled between the framers and the banks of DSPs. In general, a plurality of TSIs can also be used in system 100 for switching a time slot from the incoming TDM stream to a different time slot of the outgoing TDM stream.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ a controller for setting up and tearing down a call connection, and time slot interchangers as taught by the admitted prior art in figure 3 of the instant application into the system of Yamashita with the motivation is that to control a call's establishment and a call's ending and any time slot of an incoming TDM frame could be connected to a different time slot of an outgoing TDM stream in order to meet the required speed and efficiency of a telecommunication network.

Regarding claims 17-19, these claims have similar limitations as claims 2-4. Therefore, they are rejected under Yamashita and the admitted prior art in figure 3 of the instant application for the same reasons set forth in the rejection of claims 2-4, respectively.

Regarding claims 21-23, these claims have similar limitations as claims 16-18. Therefore, they are rejected under Yamashita and the admitted prior art in figure 3 of the instant application for the same reasons set forth in the rejection of claims 16-18, respectively.

Regarding claims 25-28, these claims have similar limitations as claims 16-19. Therefore, they are rejected under Yamashita and the admitted prior art in figure 3 of the instant application for the same reasons set forth in the rejection of claims 16-19, respectively

5. Claims 5, 14, 20, 24, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamashita, in view of the admitted prior art in figure 1 of the instant application, and further in view of Bull et al. (US 4,523,308), hereinafter referred to as Bull.

Regarding claims 5, 14, 20, 24, and 29, Yamashita and the admitted prior art in figure 3 of the instant application disclose all claimed limitations except

a step of generating an error flag if the test data is different from the transferred test data.

Bull discloses a telephone concentrator switch arrangement. The line switch controller 36-fig. 1 determines a path for transferring the digitized voice information between the subscriber line 28a-28n (FIG. 1), and central office 10 over a port group highway, a line group highway, and a time slot through the line group highway switch 38, column 10, lines 22-27. If a voice path could not be located, the line switch controller sets a program return status to "no path available" and returns to the calling program. If a voice path located, the line switch controller monitors the DONE bit (fig. 5 D) of the status register, and if the DONE bit is not set within a specific time-out period, the line switch controller sets an error flag, column 13, lines 1-22.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ a mechanism generating an error flag by a controller as taught by Bull into the system of Yamashita and the admitted prior art in figure 3 of the instant application so that if a mismatch is detected, the check circuit as a part of the testing circuitry would set an error flag and the network management system 33 would be notified of this fact for correction.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Yamashita, in view of the admitted prior art in figure 3 of the instant application, and further in view of Koenig et al.(6,351,452), hereinafter referred to as Koenig.

Regarding claim 15, Yamashita and the admitted prior art in figure 3 of the instant application disclose all claimed limitations, except the logic circuit comprises a field programmable gate array.

The FPGA is well known in the art for containing many circuits whose interconnections and functions are programmable by the user.

Koenig discloses a telecommunication device with centralized processing redundancy protection, and on-demand insertion of signaling bits, in which the controller 26-fig. 3 of the device 10-fig. 2 includes an FPGA device 112 (column 10, lines 46-54).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to employ an FPGA as taught by Keoning into the combination system of Yamashita and the admitted prior art in figure 3 of the instant application with the motivation is that the many circuits and whose interconnections and functions are programmable by the user of the FPGA would make the cross-connect system process the data at a rapid rate, and therefore the required speed and efficiency of telecommunication networks is increasing.

Allowable Subject Matter

7. Claims 6-9, and 30-37 are allowed.

Reason for allowance

8. Regarding claims 6-9, and 30-37, the prior art fails to teach or suggest a method for testing a DSP of a transmission system, the method comprises the step of generating a test signal, wherein the test signal is generated by the DSP, and inserting the test signal in one or more of the plurality unused fields of the TDM stream, in combination with other limitations, as specified in claims 6, 30, and 34.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Ho whose telephone number is (703) 305-1332. The examiner can normally be reached on Monday through Friday from 7:00 am to 3:30 pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (703) 308-6602.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA, Sixth Floor (Receptionist).

Patent Examiner

Duc Ho

06-11-03